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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,173	06/30/2003	SHI-HSIANG LU	10873-US-PA	1172
31561	7590 11/27/2006		EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE 7 FLOOR-1, NO. 100			WU, XIAO MIN	
	Γ ROAD, SECTION 2		. ART UNIT	PAPER NUMBER
TAIPEI, 10	00		2629	•
TAIWAN			DATE MAILED: 11/27/200	5

Please find below and/or attached an Office communication concerning this application or proceeding.

,	Application No.	Applicant(s)					
Office Andieus Occurrence	10/604,173	LU ET AL.					
Office Action Summary	Examiner	Art Unit					
	XIAO M. WU	2629					
The MAILING DATE of this communication Period for Reply	appears on the cover sheet w	ith the correspondence ad	dress				
A SHORTENED STATUTORY PERIOD FOR RE WHICHEVER IS LONGER, FROM THE MAILING - Extensions of time may be available under the provisions of 37 CFF after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period for reply within the set or extended period for reply will, by stany reply received by the Office later than three months after the mearned patent term adjustment. See 37 CFR 1.704(b).	B DATE OF THIS COMMUNI R 1.136(a). In no event, however, may a . riod will apply and will expire SIX (6) MOI atute, cause the application to become A	CATION. reply be timely filed NTHS from the mailing date of this co BANDONED (35 U.S.C. § 133).	,				
Status			•				
1) Responsive to communication(s) filed on 2	5 Sentember 2006						
<u> </u>	This action is non-final.						
· · · · · · · · · · · · · · · · · · ·	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice under			morns is				
Disposition of Claims	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	,					
4)⊠ Claim(s) <u>1-15</u> is/are pending in the applicat	ion						
	4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1-15</u> is/are rejected.	· <u></u>						
7) Claim(s) is/are objected to.							
	Claim(s) are subject to restriction and/or election requirement.						
Application Papers	. •						
•	almag						
9) The specification is objected to by the Examiner.							
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11) The oath or declaration is objected to by the							
Priority under 35 U.S.C. § 119	- Examinor. Note the attache		0-102.				
<u> </u>							
2) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).							
· _ ·	a) All b) Some * c) None of:						
<u> </u>	1. Certified copies of the priority documents have been received.						
 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage 							
application from the International Bur		received in this National	Stage				
* See the attached detailed Office action for a	` ' ' '	received					
	iot of the definited doples had	Teodived.					
•							
Attachment(s)							
1) Notice of References Cited (PTO-892)		Summary (PTO-413)					
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) 		s)/Mail Date nformal Patent Application					
Paper No(s)/Mail Date	6) Other:						

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1-8, 10-13 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Kihara et al. (US Patent No. 5,889,504).

As to claim 1, Kihara discloses a display driving circuit (Fig. 4), comprising: a plurality of driving stages (11, Fig. 7), wherein the driving stages are electrically coupled in serial, (see Fig. 7) and each of the driving stages comprises a conducting path so as to transmit an electric signal from a previous driving stage to a next driving stage (e.g. right normal shift register); and a plurality of driving lines (e.g. the column line 1 to each pixel cell), wherein each of the driving lines corresponds to one of the driving stages respectively (see Fig. 7), and the driving line is electrically coupled to an output terminal of a corresponding driving stage (Fig. 7); a plurality of redundant devices (e.g. right redundant shift registers) installed in part of the driving stages (11, Fig. 7), respectively, and the redundant device is capable of supplying an extra conducting path to transmit an electric signal from the previous driving stage to the next driving stage via the current driving stage while the original conducting path in the corresponding driving stage is broken (e.g. when the normal shift register is broken) wherein the driving stages (11, 11, ...Fig. 7) are electrically connected in series with the driving stage installed with the redundant devices (e.g. the driving stages 11 are connected in series through the switch circuit S1 and driving stages

11 are installed with the redundant devices SR4, see Fig. 7).

As to claim 2, Kihara discloses each of the redundant device (e.g. right redundant circuit as shown in Fig. 4) is added into a driving stage subsequent to a plurality of preceding driving stages that are installed separately departing from a predetermined number of the driving stages with each other (see Fig. 4).

As to claim 3, Kihara discloses each of the redundant device (e.g. right redundant circuit as shown in Fig. 4) is added to a plurality of contiguous driving stages subsequent to a predetermined number of the driving stages with each other (see Fig. 4).

As to claims 4, 10, Kihara discloses a display driving circuit, comprising: a plurality of driving stages (11-14, Fig. 4), electrically coupled in serial; a plurality of redundant stages (e.g. SR2 and SR4), alternatively disposed between the driving stages (SR1, SR3) and electrically coupled to adjacent driving stages, and each of the redundant stage comprises a conducting path so as to transmit an electric signal from the previous driving stage to the next driving stage, wherein the redundant stage (SR43 of the first stage 11 in Fig. 7) and the driving stage (SR3 of the following stage 11 in Fig. 7) are electrically connected in serial (e.g. when the right SR3 is not performing the normal shifting operation, on the other hand, the switch circuit 71 controls the transmission gates 72 and 73 so that the gate 72 is turned off while the gate 73 is turned on. As a result, the data signal from the right redundant register SR4 is supplied via the transmission gate 73 to the right normal register SR3 and the right redundant register SR4 of the shift register group 11 of the next stage, see col. 9, lines 19-27); and a plurality of driving lines, wherein each of the driving lines (e.g. the column line 1 to each pixel cell) corresponds to one of the driving stages or the redundant stages respectively, and each of the driving line is electrically

coupled to an output terminal of a corresponding driving stage or a corresponding redundant stage (e.g. when the normal shift register is broken)..

As to claims 5, 11, Kihara discloses each of the redundant stage (e.g. RB3, Fig. 4) includes a driving stage (SR1, SR3) and a redundant device (SR2, SR4).

As to claims 6, 12, Kihara discloses each pair of two adjacent redundant stages (e.g. two adjacent SR4s) further comprises at least one another driving stage (SR3) electrically coupled there between.

As to claims 7, 13, Kihara discloses the redundant device comprises a plurality of transistors (72, 73, Fig. 7) in the driving stage.

As to claims 8, 14, Kihara discloses the redundant device is capable of supplying an extra conducting path to transmit an electrical signal from the previous driving stage to the next driving stage via the current redundant stage while the original conducting path in the corresponding path in the corresponding driving stage of the redundant stage is broken. (col. 9, lines 3-36).

As to claim 15, Kihara discloses the driving stage group includes N number of t a plurality of driving stages, and the redundant stage is electrically connected subsequent to the driving stage group (see Figs. 4 and 7).

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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- 4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
- 5. Claims 9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kihara et al. (US Patent No. 5,889,504).

As to claims 9 and 14, Kihara shows four transistors (72, 73) and a switching circuit (71 and a plurality of invertors in the driving stage. Kihara does not specifically discloses that there are total six transistors in the driving stage. However, it would have been obvious to one of ordinary skill in the to have realized that more than four transistors could be integrated into the driving stage since the switch circuit or the invertors could also include transistors.

Response to Arguments

6. Applicant's arguments filed 6/7/2006have been fully considered but they are not persuasive.

With respect to claim 1, applicant argues that the prior art to Kihara does not disclose the newly added limitations of "wherein the driving stages are electrically connected in series with the driving stages installed with the redundant devices" as recited in claim 1. This argument is not persuasive because Fig. 7 of Kihara clearly shows that the driving stages 11 are connected in

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series through the switch circuit S1 and driving stages 11 are installed with the redundant devices SR4).

With respect to claims 4 and 10, applicant also argues that Kihara does not disclose the newly added limitations of "wherein the redundant stage and the driving stage are electrically connected in serial" as recited in claims 4 and 10. This argument is not persuasive because Kihara clearly discloses that when the right SR3 is not performing the normal shifting operation, on the other hand, the switch circuit 71 controls the transmission gates 72 and 73 so' that the gate 72 is turned off while the gate 73 is turned on. As a result, the data signal from **the right redundant register SR4** is supplied via the transmission gate 73 **to the right normal register** SR3 and the right redundant register SR4 of the shift register group 11 of the next stage. In other words, the right redundant stage SR4 of the previous stage is connected in serial with the right normal register stage SR3 (see col. 9, lines 19-27).

Conclusion

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to XIAO M. WU whose telephone number is 571-272-7761. The examiner can normally be reached on 6:30 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RICHARD HJERPE, can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

x.w.

November 18, 2006

XIAO M. WU

Supervisory Patent Examiner

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